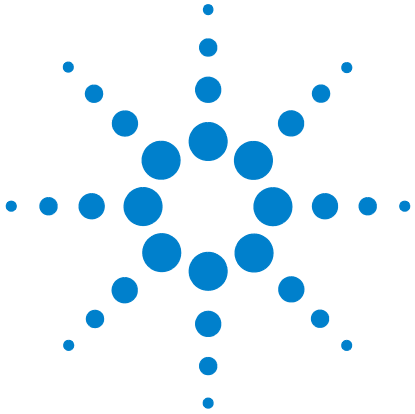

Agilent Midbus Series 2.0 of Probes using Soft Touch Technology

User Guide

Agilent Technologies

Notices

Installation Guides

You can find the installation guides for different components of the product on the product CD. Agilent recommends you to do not switch on the instrument before you have understood all the applicable installation instructions and have met all the installation prerequisites.

Where to find more information

You can find more information about Protocol Analyzer from the following link:

http://www.agilent.com/find/spt

You can also look for search a local contact for assistance on the following link

http://www.agilent.com/find/assist

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Frame or chassis ground terminal. Typically connects to the equipment's metal frame.

Indicates hazardous voltages and potential for electrical shock.

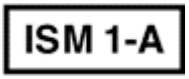
Indicates that antistatic precautions should be taken.

Indicates hot surface. Please do not touch.

Indicates laser radiation turned on.

Safety requirements for electrical equipment for measurement, control, and laboratory use CAN/CSA C22.2 No. 1010.1 (1993) UL 3101, 3111 (First Editions) This equipment has also been evaluated to IEC 61010 edition 1 including amendments 1 and 2.

Notice for European Community: This product complies with the relevant European legal Directives: EMC Directive 89/336/EEC and Low Voltage Directive 73/23/EEC.



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This product complies with the WEEE Directive (2002/96/EC) marking requirements. The affixed label indicates that you must not discard this electrical/ electronic product in domestic household waste.

Product Category: With reference to the equipment types in the WEEE Directive Annex I, this product is classed as a "Monitoring and Control instrumentation" product.

Do not dispose in domestic household waste.

To return unwanted products, contact your local Agilent office, or see www.agilent.com/environment/product/ for more information.

Contents

1
Introduction

This chapter introduces you to Agilent midbus 2.0 series of probes using soft touch technology. It also provides information on configuration support for it.

Objectives

The Agilent midbus 2.0 series of probes using soft touch technology are specially designed to provide support for up to 16 channel probing solutions.

To integrate a midbus probe, a midbus probe footprint must be designed into the target board. A 3 pin header must also be designed into the target board if it is required to supply a reference clock to the protocol analyzer. This document is intended to provide information needed by platform and system design teams for integration of midbus 2.0 into their designs. It provides a mechanical and electrical solution space for Midbus Probe placement with the PCI Express bus.

Although information on PCI Express topology and specifications will be given, this document is not intended to take the place of other PCI Express design documentation. It is assumed that a design team utilizing this document for their design constraints will validate their designs through pre and post route electrical simulation and keep- out volume analysis.

Nomenclature

- N4241A refers to midbus 2.0 straight bi- directional x8 for PCIe 5 Gb/s.
- N4242A refers to midbus 2.0 swizzled x16 for PCIe 5Gb/s.
- N4243A refers to midbus 2.0 split x4 for PCIe 5Gb/s.
- Midbus connection, midbus probe, and midbus footprint refer to the Agilent midbus 2.0 footprint connector (N4241A/ N4242A/ N4243A) PCI Express compression cable set.
- “channel” refers to either an upstream differential pair OR downstream differential pair for a given lane. In other words, a “channel” refers to either a transmit- differential pair OR a receive- differential pair for a given lane.

Retention modules:

One kit of 5 retention modules is supplied with each N4241A, N4242A, and N4243A probes.

Additional kits for them can be ordered by using Agilent part number N4241- 68702 (PI:600- 0195- 00).

For larger quantities, please contact Precision Interconnect at: 10025 SW Freeman Ct., Wilsonville, OK 97070 (503- 685- 9300). http://www.precisionint.com

Overview and Configuration Support

Figure 1 Agilent Midbus 2.0

Link configuration support

The midbus 2.0 offers a number of different probing options for different applications. The platform designer has the flexibility to configure a probing solution that best meets the needs of the system. With midbus 2.0 offering upto 16 channel probing solutions, the following configurations may be made*:

- Upstream and downstream channels of one x8 link.
- Upstream or downstream channels of one x16 link.
- Upstream or downstream channels of up to four x4, x2, or x1 links.

* As long as the Midbus Probe placement within the system requirements are met. System designers should verify that their system requirements are supported by the midbus 2.0 by contacting Agilent Technologies directly.

NOTE Other combinations may be available. Contact Agilent Technologies for the latest support configurations.

Installation Instructions

- First solder and secure the retention module onto the device under test (DUT) on two sides of the midbus probe footprint.
- Select the midbus cable (straight, swizzle or split) that best suits the design. Connect the wide connector of midbus to the Protocol Analyzer module and tighten the thumbscrews.
- Identify the white bullet on the probe label indicating pin 1 as seen in Figure 1. Align it to the pin 1 on the layout board. (While designing the layout make sure pin 1 is defined and marked.) A vertically aligned probe is shown in the Figure 2.
- Slide the probe into the retention module and gently tighten the thumbscrews located at the top of the midbus probe head. A screwdriver may be used to ensure that there is a secure connection. The thumbscrews should be tightened to a snug fit but do not over tighten.

Figure 2 midbus aligned over back plane

- Finally, if an external reference clock is to be supplied to protocol analyzer, connect the external clock cable (of the midbus) to the reference clock header on the target board.

Specifications

CAUTION Please read the specifications stated below carefully before setting up the design for midbus.

Probe Inputs:

- Input Voltage: 25V max or 3V rms into 250 Ohms.

Temperature:

- Operating 0 to 40 Deg C with 200 linear feet per minute airflow.
- Storage - 40 to 70 Deg C.

Humidity:

- Operating 15% to 95% non condensing.

Altitude:

- Operating: to 3000 meters (10000 ft).

Airflow:

- For a single probe with no heat sources within 1 inch, 140 linear feet per minute of air flow is required.
- For two probes, placed side by side with minimum spacing and no other heat sources within 1 inch, 200 linear feet per minute of air flow is required.

Reference clock

For many solution setups an external reference clock is not required. However, if any of the following cases are true then an external reference clock must be supplied for each PCI Express clock domain for which the case applies.

• When the midbus probe is used with a system that supports Spread Spectrum Clocking (SSC) on the reference clock to all the PCI Express agents and the SSC can not be disabled

• When testing must be done with SSC enabled, because a problem does not manifest with SSC disabled.

• If the link frequency is intentionally margin tested outside the standard ±300 ppm tolerance.

NOTE This is more restrictive than the PCI Express standard of ±300 ppm, but must be considered. For more information, contact Agilent Technologies directly.

The reference clock can be a dedicated clock, in which case appropriate terminators must be provided on the board. Alternately, the signals may be a tap off an existing clock, since the probes are designed to not significantly load the signals. Note that if the reference clock signal is series/source terminated then the position of the tap point must be at the far end of the line. However, this needs to be verified by the system platform designers to verify proper functionality. See reference clock model (Figure 13) for more information.

2
Mechanical Design

This section contains information on mechanical design of the Midbus Probe and the reference clock pin header. It also provides details on footprint dimensions, keep- out volumes, and part numbers.

Footprint dimensions and specifications

Please ensure the following pre- requisites are met for the design:

- Solder mask must not extend above the pad height for a distance of .005 inches from the pad.
- Via- in- pad is allowed if the vias are filled level with the pad or the via hole size is less that .005 inches.
- Permissible surface finishes on pads are HASL, immersion silver, or gold over nickel. The height of the pads contacted by the probe must be within +/- .007 inches of the bottom surface of the retention module.

The midbus probe 2.0 footprint, that needs to be designed into the target board can be observed in Figure 3. The figure displays the detailed layout dimensions for the footprint. Notice that the connector has 50 pins.

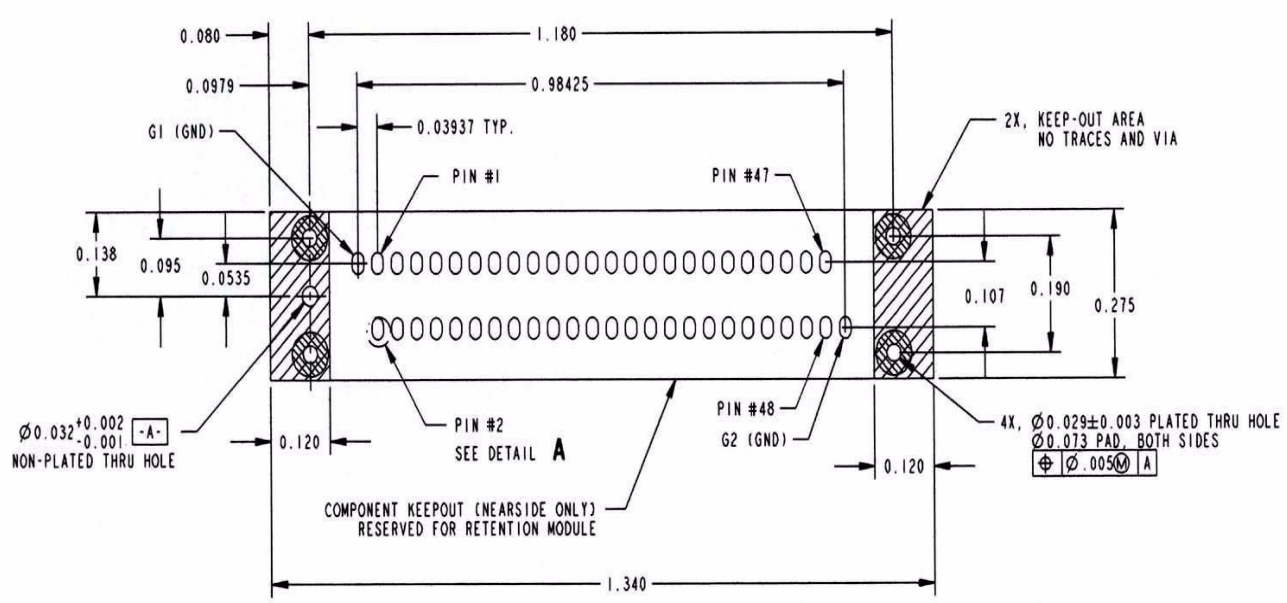

Figure 3 midbus 2.0 footprint dimensions, pin numbering, and specification

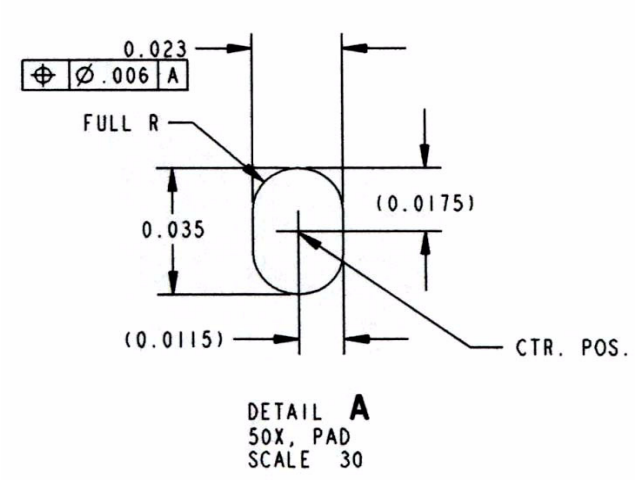

Figure 4 Detail A: detailed view of a pad.

Figure 4 displays detailed view of a pad with geometrical information on it.

Connecting the Retention Module

The retention module helps to connect midbus probe to the device under test (DUT). To achieve this, the retention module must be soldered onto the DUT. After this is done, the probe can be easily plugged into this retention module. Figure 5 displays dimensions of the midbus plugged into the retention module.

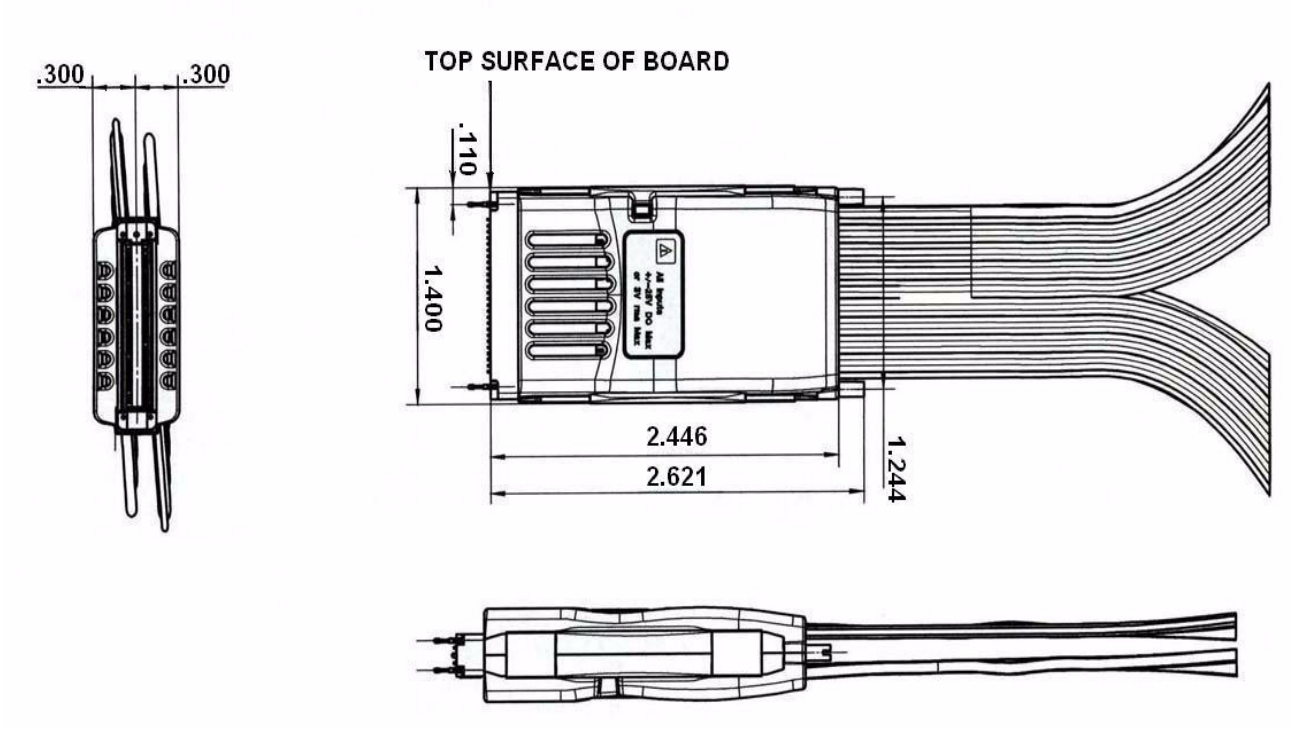

Figure 5 Midbus probe plugged into the retention module .

The detailed specifications of the retainer can be observed in Figure 6

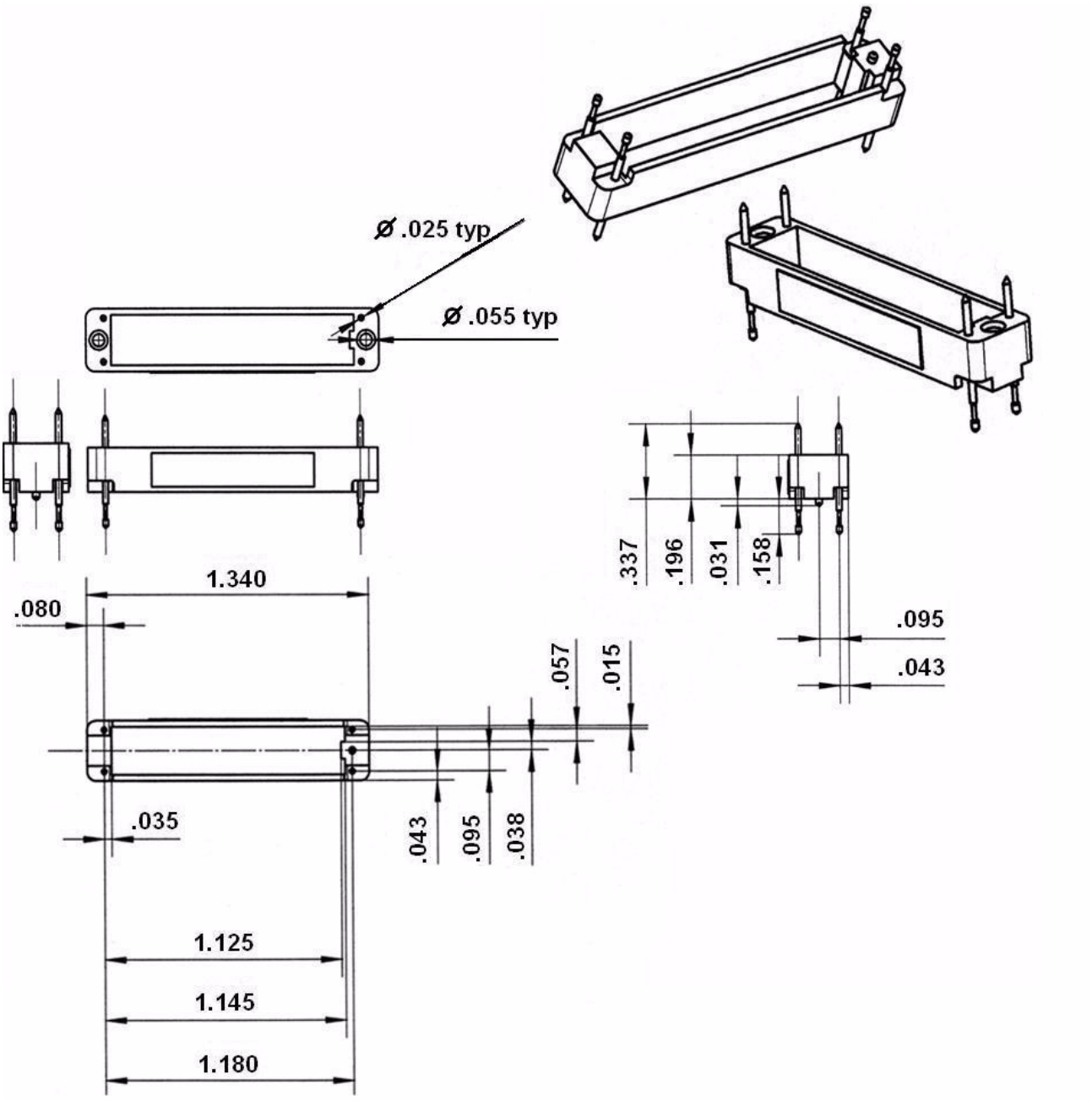

Figure 6 Retention module specifications

Reference clock

Reference clock header

A 3- pin header (1 by 3, 0.05 inch center spacing) will provide the connection for reference clock to the midbus. A small high impedance clock probe will connect to this header to the midbus. Note that an individual reference lock header is required for each PCI Express clock domain on the system.

The following are recommended part numbers for through- hole and surface mount versions of the 3- pin header for reference clock:

- Through- hole:

Samtec* TMS- 103- 02- S- S

- Surface mount:

Samtec* FTR- 103- 02- S- S

Table 1 Reference clock header pinout

Signal	Pin Number
REFCLKp	1 (or 3)*
GND or N/C	2
REFCLKn	3 (or 1)*

* The probe can be plugged onto the pin header in either orientation.

Reference clock probe keep-out volume

Keep- out volumes for the reference clock probes are given in Figure 7. The pin headers reside symmetrically within the keep- out volume on the target system. For more specific information on keep- out volumes for particular solutions please contact Agilent Technologies.

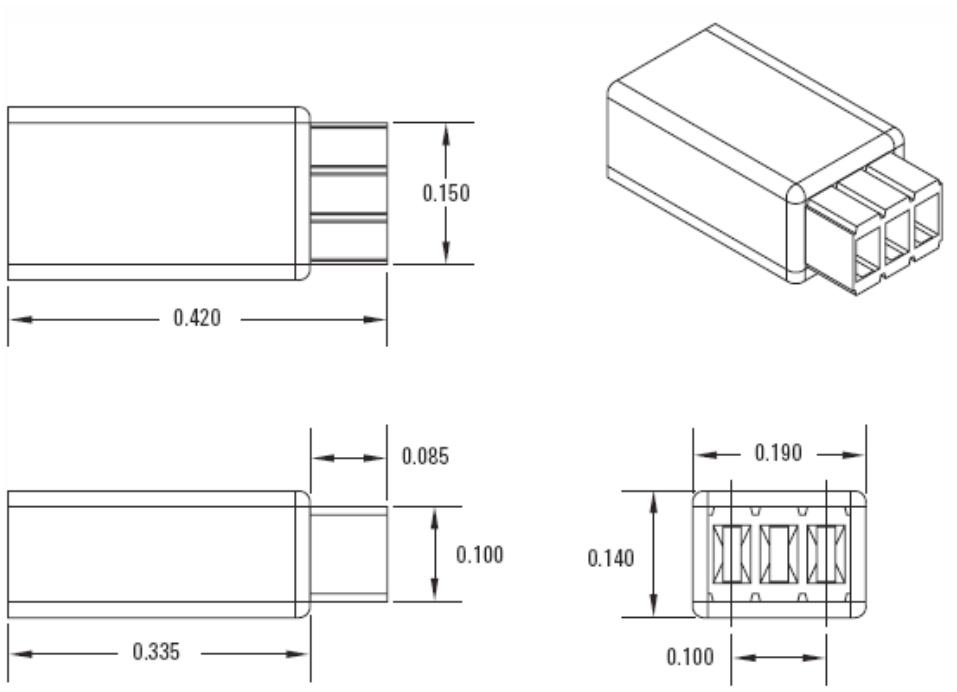

Figure 7 Reference clock probe keep-out volume

3
Electrical Design

This section contains electrical design details and reference clock pin header of the midbus 2.0 series of probes using soft touch technology. These details include analyzer eye requirement definition, system impact due to midbus probe presence, midbus routing suggestions, load models, and pin assignments.

Midbus 2.0

Logical probing of the PCI Express bus is achieved through tapping a small amount of energy off the probed signals and channeling this energy to the logic analyzer. In order to avoid excessive loading conditions, the use of tip resistors, or isolation resistors, is employed. These relatively high impedance tip resistors enable the logic analyzer to sample bus traffic without significantly loading the probed signals. A high- level block diagram of a generic PCI Express bus with a logic analyzer interface is given in Figure 8. Note that this would be repeated for each differential pair within a PCI Express link.

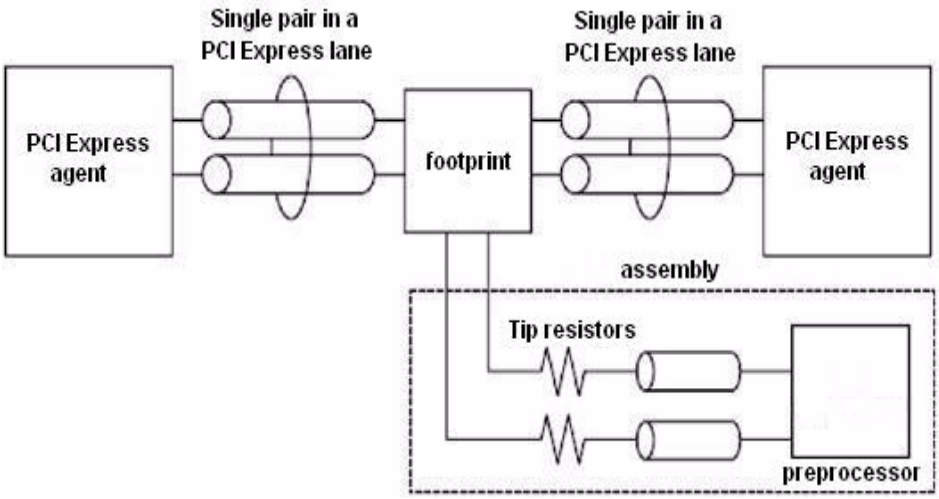

Figure 8 Block diagram example of a generic PCI Express bus with a protocol analyzer.

Midbus placement within system topology

In order for the analyzer to reliably capture logical transactions on the bus, adequate signal eye must be made available to the midbus. It is incumbent upon the platform designers to ensure that sufficient signal eye is available to the midbus while the midbus load is in place so that proper signal capture can be performed. This must be verified via electrical simulation utilizing the load model provided in Figure 12.

The eye requirements are measured by eye height and eye width, forming a diamond shape. These requirements are described pictorially in Figure 9.

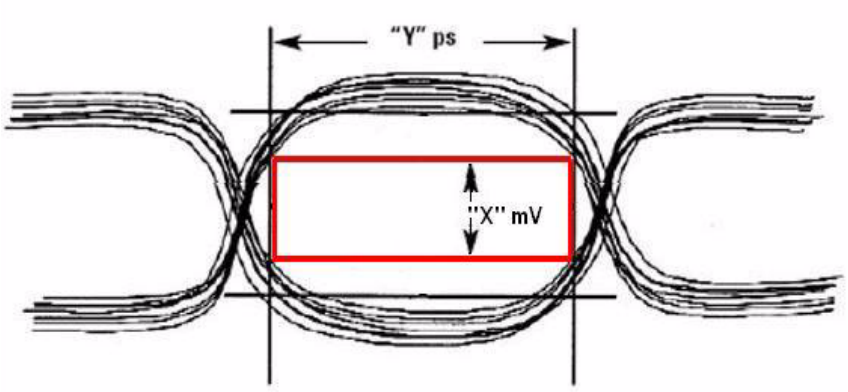

Figure 9 Example of eye specifications as seen at the midbus pad

Table 2 details the specific eye requirements for Agilent Technologies. Address questions to Agilent Technologies for the most current eye requirements.

Table 2 PCI Express midbus footprint placement interconnect specification

	Agilent Technologies Specification
Min. eye height at midbus pad[1]	60 mV
Min. eye width at midbus pad	0.6 UI (120 ps at midbus footprint), i.e. Jitter tolerance of 0.4 UI
Length matching requirements of the P/N sides of the differential pairs[2]	±5 mil
Length matching requirements -pair to pair	same as PCI Express specification

1 Measured in differential units, e.g. Vppdiff = |2*(Vp – Vn)|

2 Interconnect must length match ±5 mils from source to midbus footprint pad for each polarity of the differential pair.

The eye characteristics given in Table 2 must be maintained for all probed channels, regardless of direction. Overall, these midbus placement specifications limit the electrical distance between the driver pin and the midbus attach point. Conceivably, probing both directions in lanes of a long PCI Express link may require two separate footprints and midbus assemblies, while probing both directions of relatively short links may be accomplished with one midbus. Regardless of implementation, refer to usage restrictions as listed in the

"Overview and Configuration Support" section. The same midbus eye requirements exist for all links substrates (e.g. FR4, cables, etc.).

An additional constraint on midbus footprint placement involves the relative location of the AC coupling capacitors. The capacitors may be placed either between the driver and midbus, or between the midbus and receiver, as long as both capacitors of a differential pair are placed in the same fashion. Other pairs within a link do not need to maintain this capacitor placement configuration.

Routing considerations near/through PCI Express midbus footprint

Agilent will provide detailed information on routing and design considerations at a later date. Figure 8 presents suggested routing for footprint negotiation in the case of surface (microstrip) routing when this routing is on the same side of the board as midbus.

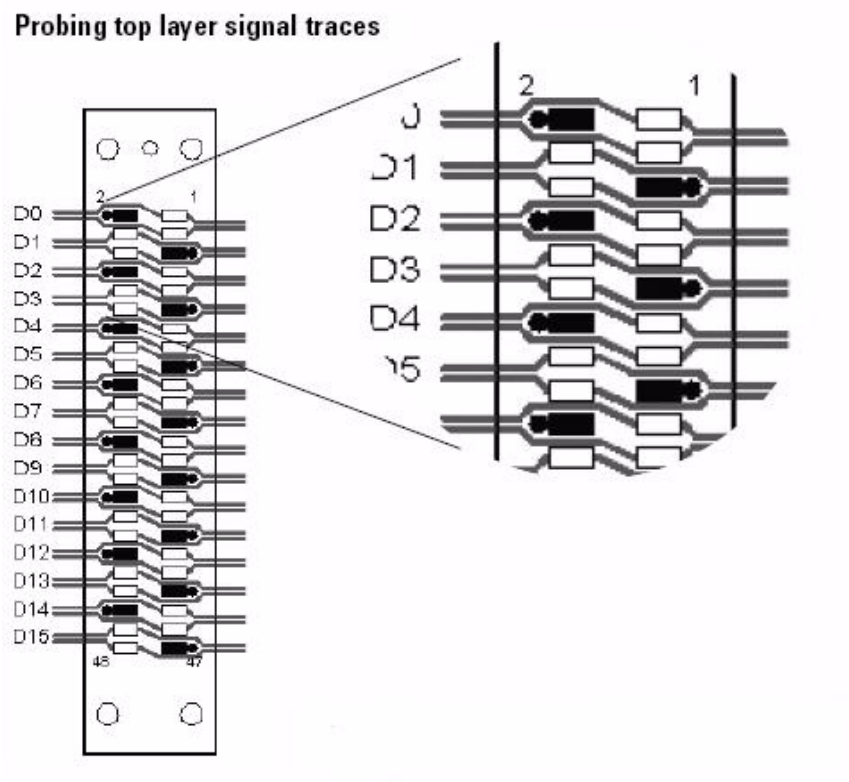

Figure 10 Suggested routing for microstrip traces on same layer as midbus

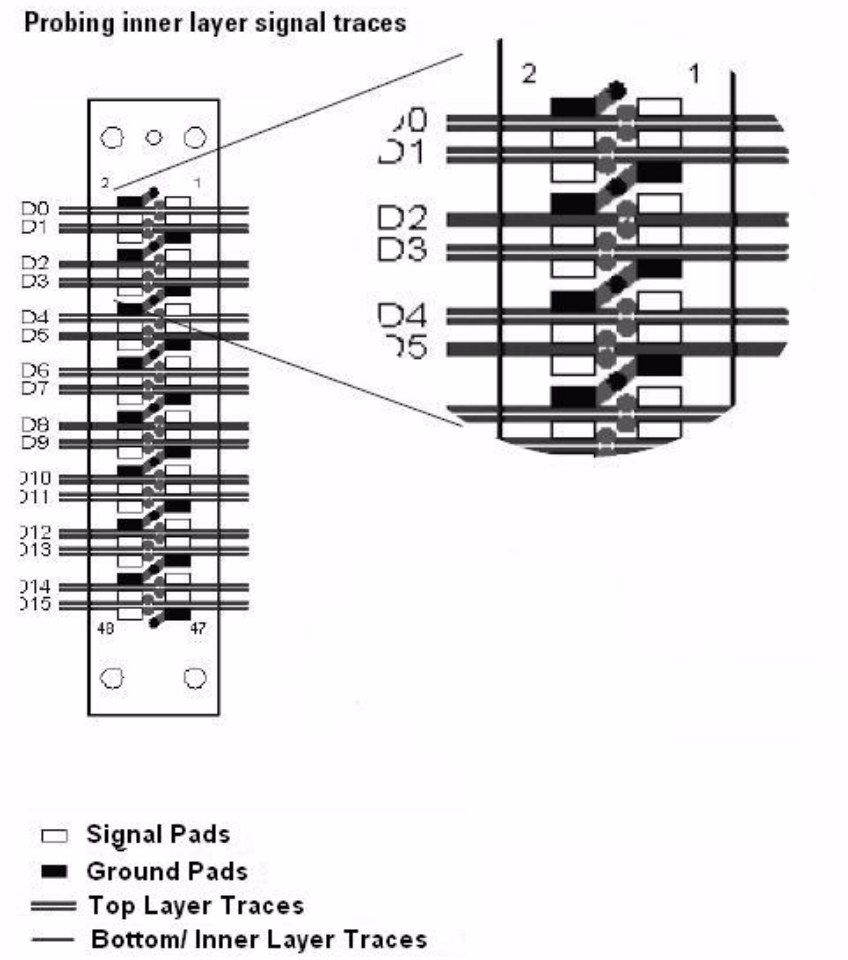

Figure 11 Inner layer and secondary side routing (surface layer opposite of midbus)

Load Models

Agilent Technologies* Load Model

The Agilent Technologies load model for the midbus is given in Figure 10. This model is subject to change. For the most current models, it is recommended that the platform designer contact Agilent Technologies directly.

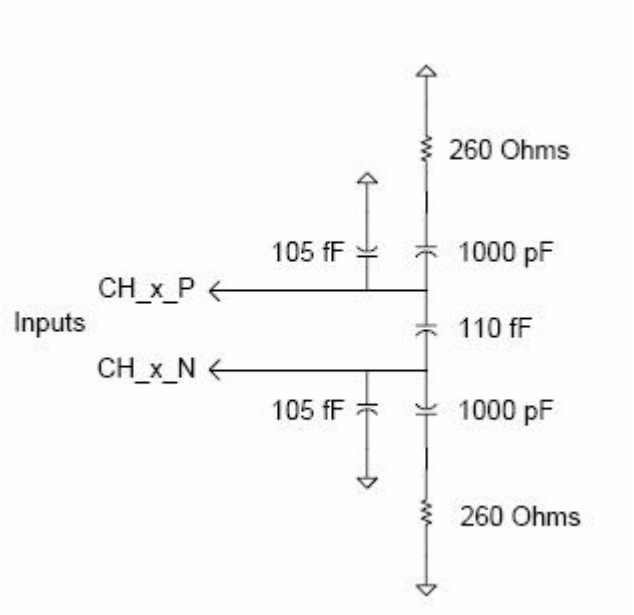

Figure 12 Load model for midbus probe

PCI Express midbus pin assignments

There is flexibility in the arrangement and layout of the midbus footprint. Agilent will provide configuration of the midbus to support the following midbus layouts. There is a detailed view of these connections below.

The pinout for the PCI Express midbus is given in “Full- size midbus pin assignment, General PCI Express midbus pinout,” Table 3. It is imperative that designers understand there is some freedom associated with the pin/signal assignment relationship. These notes are given here:

Footprint channel vs.lane/link designations	• Channel = either an upstream OR downstream differential pair for a given lane • C<letter> = the designator for a Channel which accepts a given differential pair of signals • C<letter><p or n> = the two signals of the differential pair.The signals within a given pair may be assigned to either p or n regardless of polarity

General rules for signal pair assignment	The differential pairs that make up the PCI Express links must be assigned to specific pins of the footprint. However, there is some freedom in this pair assignment in order to minimize routing constraints on the platform. Additionally, note that the channel to footprint assignment configuration is closely related to the “direction” of the probed link. More specifically, a bi-directional pin assignment is different from a unidirectional pin assignment. See the following tables contained in this section for more information.

Probing Options

The PCI Express Gen2 analyzer offers three different probing options for different applications to suit different footprints on the DUT.

Full- size midbus pin assignment

In this section you will learn about full- size midbus pin assignment for:

- General
- Straight
- Swizzled x16
- Split x4

General

Table 3 General PCI Express midbus pinout

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	CAp
4	CBp	3	CAn
6	CBn	5	GND
8	GND	7	CCp
10	CDp	9	CCn
12	CDn	11	GND
14	GND	13	CEp
16	CFp	15	CEn
18	CFn	17	GND
20	GND	19	CGp
22	CHp	21	CGn
24	CHn	23	GND
26	GND	25	CIp
28	CJp	27	CIn
30	CJn	29	GND
32	GND	31	CKp
34	CLp	33	CKn
36	CLn	35	GND
38	GND	37	CMp
40	CNp	39	CMn
42	CNn	41	GND
44	GND	43	CPp
46	CQp	45	CPn
48	CQn	47	GND
G2	GND		

Straight

This type of probe connects all 16 differential pairs of one probe head to one I/O module. In case of a uni- directional pin configuration it can be used to probe a single direction of a x1...x16 link (see Table 4), and in case of bi- directional configuration it can be used to probe both directions of a x1...x8 link (see Table 5).

Table 4 x16 (standard) PCI Express midbus pinout[1, 2, 3,4]

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	C0p
4	C1p	3	C0n
6	C1n	5	GND
8	GND	7	C2p
10	C3p	9	C2n
12	C3n	11	GND
14	GND	13	C4p
16	C5p	15	C4n
18	C5n	17	GND
20	GND	19	C6p
22	C7p	21	C6n
24	C7n	23	GND
26	GND	25	C8p
28	C9p	27	C8n
30	C9n	29	GND
32	GND	31	C10p
34	C11p	33	C10n
36	C11n	35	GND
38	GND	37	C12p
40	C13p	39	C12n
42	C13n	41	GND
44	GND	43	C14p
46	C15p	45	C14n

Table 4 x16 (standard) PCI Express midbus pinout[1, 2, 3,4]

48	C15n	47	GND
G2	GND		

[1] Polarity (p and n) of each differential pair may be swapped.

[2] This configuration can only probe either upstream 16 channels OR 16 downstream channels with one midbus. Please see Table 5 for a configuration that supports interleaved x16 traffic amongst two midbus footprints.

[3] Entire link assignment may be reversed in midbus. For example, channel 0 may be swapped in above table with channel 15, channel 1 with channel 14, etc. If swapping upstream, must also swap downstream (and vice versa).

[4] Analyzer supports probing of one link with smaller link width (x1, x2, x4, x8) on natural lane boundaries, e.g. a x4 link can be probed on lanes 0...3, 4...7, 8...11 or 12...15

Table 5 x8 (straight, bi-directional) specific PCI Express midbus pinout[1, 2, 3, 4, 5]

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	C0p- Upstream
4	C0p- Downstream	3	C0n- Upstream
6	C0n- Downstream	5	GND
8	GND	7	C1p- Upstream
10	C1p- Downstream	9	C1n- Upstream
12	C1n- Downstream	11	GND
14	GND	13	C2p- Upstream
16	C2p- Downstream	15	C2n- Upstream
18	C2n- Downstream	17	GND
20	GND	19	C3p- Upstream
22	C3p- Downstream	21	C3n- Upstream
24	C3n- Downstream	23	GND
26	GND	25	C4p- Upstream
28	C4p- Downstream	27	C4n- Upstream
30	C4n- Downstream	29	GND
32	GND	31	C5p- Upstream
34	C5p- Downstream	33	C5n- Upstream
36	C5n- Downstream	35	GND

Table 5 x8 (straight, bi-directional) specific PCI Express midbus pinout[1, 2, 3, 4, 5]

38	GND	37	C6p- Upstream
40	C6p- Downstream	39	C6n- Upstream
42	C6n- Downstream	41	GND
44	GND	43	C7p- Upstream
46	C7p- Downstream	45	C7n- Upstream
48	C7n- Downstream	47	GND
G2	GND		

[1] Polarity (p and n) of each differential pair may be swapped.

[2] Can probe upstream 8 channels AND downstream 8 channels with one midbus.

[3] Entire link assignment may be reversed in midbus. For example, channel 0-upstream may be swapped in above table with channel 7-upstream, channel 1-upstream with channel 6-upstream, etc. If swapping upstream, must also swap downstream (and vice versa).

[4] Upstream and downstream pin assignments may be swapped. For example, channel 0-upstream may be swapped with channel 0-downstream, etc. Note that if one channel of upstream swapped with downstream, all channels upstream and downstream channels must be swapped.

[5] Analyzer supports probing of one bi-directional link with smaller link width (x1, x2, x4) on natural lane boundaries, e.g. a x4 link can be probed on lanes 0...3 or 4...7

Swizzled x16

This type of probe is used in cases where a x16 link is split up onto two footprints in such a way that lanes 0...7 of both directions are on one footprint and lanes 8...15 of both directions are on the other. The swizzled probe connects two probe heads to two I/O modules in a way that each of the I/O modules receives all 16 channels of one direction. The probe heads are labeled "A" and "B". The "A" probe head must be plugged into the footprint that carries lanes 0...7, whereas the "B" probe head must be plugged into the footprint that carries lanes 8...15 (see Table 6).

NOTE Probe head "B" must be plugged in 180 degrees rotated.

Table 6 Swizzled x16 PCI Express midbus pinout[1, 2, 3, 4, 5]

Midbus footprint A - lanes 0...7

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	C0p- Upstream
4	C0p- Downstream	3	C0n- Upstream
6	C0n- Downstream	5	GND
8	GND	7	C1p- Upstream
10	C1p- Downstream	9	C1n- Upstream
12	C1n- Downstream	11	GND
14	GND	13	C2p- Upstream
16	C2p- Downstream	15	C2n- Upstream
18	C2n- Downstream	17	GND
20	GND	19	C3p- Upstream
22	C3p- Downstream	21	C3n- Upstream
24	C3n- Downstream	23	GND
26	GND	25	C4p- Upstream
28	C4p- Downstream	27	C4n- Upstream
30	C4n- Downstream	29	GND

Midbus footprint B - lanes 8...15

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	C8p- Upstream
4	C8p- Downstream	3	C8n- Upstream
6	C8n- Downstream	5	GND
8	GND	7	C9p- Upstream
10	C9p- Downstream	9	C9n- Upstream
12	C9n- Downstream	11	GND
14	GND	13	C10p- Upstream
16	C10p- Downstream	15	C10n- Upstream
18	C10n- Downstream	17	GND
20	GND	19	C11p- Upstream
22	C11p- Downstream	21	C11n- Upstream
24	C11n- Downstream	23	GND
26	GND	25	C12p- Upstream
28	C12p- Downstream	27	C12n- Upstream
30	C12n- Downstream	29	GND

Table 6 Swizzled x16 PCI Express midbus pinout[1, 2, 3, 4, 5]

Midbus footprint A - lanes 0...7				Midbus footprint B - lanes 8...15			
Pin #	**Signal Name**	**Pin #**	**Signal Name**	**Pin #**	**Signal Name**	**Pin #**	**Signal Name**
32	GND	31	C5p- Upstream	32	GND	31	C13p- Upstream
34	C5p- Downstream	33	C5n- Upstream	34	C13p- Downstream	33	C13n- Upstream
36	C5n- Downstream	35	GND	36	C13n- Downstream	35	GND
38	GND	37	C6p- Upstream	38	GND	37	C14p- Upstream
40	C6p- Downstream	39	C6n- Upstream	40	C14p- Downstream	39	C14n- Upstream
42	C6n- Downstream	41		42	C14n- Downstream	41	GND
44	GND	43	C7p- Upstream	44	GND	43	C15p- Upstream
46	C7p- Downstream	45	C7n- Upstream	46	C15p- Downstream	45	C15n- Upstream
48	C7n- Downstream	47	GND	48	C15n- Downstream	47	GND
G2	GND			G2			

[1] Polarity (p and n) of each differential pair may be swapped.

[2] Can probe upstream 16 channels and downstream 16 channels with swizzled x16 probe.

[3] Entire link assignment may be reversed in midbus. For example, channel 0-upstream may be swapped in above table with channel 7-upstream, channel 1-upstream with channel 6-upstream, etc. If swapping upstream, must also swap downstream (and vice versa) and if swapping footprint A, must also swap footprint B.

[4] Upstream and downstream pin assignments may be swapped. For example, channel 0-upstream may be swapped with channel 0-downstream, etc. Note that if one channel of upstream swapped with downstream, all channels upstream and downstream channels must be swapped.

[5] Analyzer supports probing of one bi-directional link with smaller link width (x1, x2, x4, x8) on natural lane boundaries, e.g. a x4 link can be probed on lanes 0...3, 4...7, 8...11 or 12...15

Split x4

This type of probe is used to probe two bi- directional x1...x4 links on the same footprint simultaneously. The split x4 probe connects one probe head to two I/O modules in such a way that each I/O module analyzes one of the bi- directional links (see Table 8).

Table 7 Dual x4 (bi-directional)

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	C0p- Upstream1
4	C0p- Downstream1	3	C0n- Upstream1
6	C0n- Downstream1	5	GND
8	GND	7	C1p- Upstream1
10	C1p- Downstream1	9	C1n- Upstream1
12	C1n- Downstream1	11	GND
14	GND	13	C2p- Upstream1
16	C2p- Downstream1	15	C2n- Upstream1
18	C2n- Downstream1	17	GND
20	GND	19	C3p- Upstream1
22	C3p- Downstream1	21	C3n- Upstream1
24	C3n- Downstream1	23	GND
26	GND	25	C0p- Upstream2
28	C0p- Downstream2	27	C0n- Upstream2
30	C0n- Downstream2	29	GND
32	GND	31	C1p- Upstream2
34	C1p- Downstream2	33	C1n- Upstream2
36	C1n- Downstream2	35	GND
38	GND	37	C2p- Upstream2
40	C2p- Downstream2	39	C2n- Upstream2
42	C2n- Downstream2	41	GND
44	GND	43	C3p- Upstream2
46	C3p- Downstream2	45	C3n- Upstream2
48	C3n- Downstream2	47	GND
G2	GND		

Reference Clock

Table 8 Midbus reference clock electrical requirements

Midbus Requirement	Symbol	Min.	Max.	Comments
Differential voltage at ref clock attach point	Vppdiff	0.8 V	2 V	Vppdiff = |2*(Vrefclockp – Vrefclockn)|
Reference clock frequency without SSC	f	100 MHz -300 ppm	100 MHz +300 ppm	
Reference clock frequency with SSC	f	100 MHz -0.5%	100 MHz +0%	

If reference clock tolerance is less than ±300 ppm, there is no need for providing reference to the midbus. If the reference clock tolerance is greater than ±300 ppm, there is a need for providing reference (SSC) to the midbus.

midbus reference clock probe load model

Load models for the reference clock probe are given in this section. System designers will be expected to perform simulations of the reference clock networks with the header and midbus load models to ensure good signal integrity of the reference clocks at the header to the midbus. The pin header parasitics may be obtained from the connector vendor.

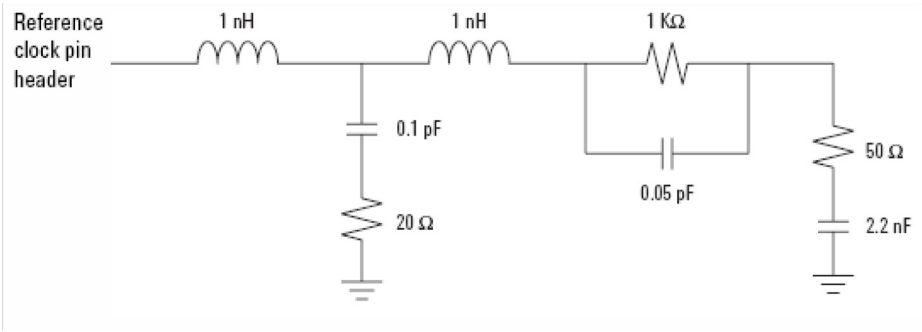

Figure 13 Reference clock probe load model

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